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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,053	12/20/2001	Dana L. Rose	30320/37779	2228

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,053	ROSE ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 08/31/2005. These drawings are accepted.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "a bit stream comparison unit **to compare** a first bit value sequence of the received bit stream to a second bit value sequence associated with a transmitted bit stream" [Emphasis Added]. Claim 1 recites, "a multi-source agreement compliant electrical connector **to convey** the transmitted and received bit streams" [Emphasis Added]. The subjunctive mood or conjugation in Grammar is indefinite. The Examiner assumes the following was intended: --a bit stream comparison unit **that compares** a first bit value sequence of the received bit stream to a second bit value sequence associated with a transmitted bit stream--. The Examiner assumes the following was intended: --a multi-source agreement compliant electrical connector **conveying** the transmitted and received bit streams--.

Response to Arguments

3. Applicant's arguments filed 08/31/2005 have been fully considered but they are not persuasive.

The Applicant contends, "that Murata does not teach a multi-source agreement compliant electrical connector, as recited in claim 1, or any type of connector whatsoever. On the contrary, Murata teaches sending and receiving circuits (1) and (2), neither of which can be fairly construed to be connectors".
The Examiner disagrees and asserts that and asserts that The Authoritative Dictionary of IEEE Standards Terms defines connector as a coupling device employed to connect conductors of one circuit or transmission element with those of another circuit or transmission element. Sending and receiving circuits (1) and (2) in Figure 1 of Murata connect electrical circuitry within Tester 10 to various transmission elements outside of Tester 10 including DSU 24 in Figure 1; hence Sending and receiving circuits (1) and (2) in Figure 1 of Murata are a connector.

The Applicant contends, "Further, although Murata teaches that the sending circuit (1) is connected to T-lines (21) and that the receiving circuit (2) is connected to R-lines (22), Murata fails to teach any type of connector that is used to make the connections, much less a multi-source agreement compliant electrical connector as recited in claim 1. Moreover, the T-lines (21) and the

Rlines (22) are not a multi-source agreement compliant device, but are instead cables or transmission lines".

The Examiner disagrees and asserts that Murata teaches a bit stream comparison unit **that compares** a first bit value sequence of the received bit stream to a second bit value sequence associated with a transmitted bit stream to detect a sequence difference between the first and second bit value sequences (the Abstract in Murata teaches that the Error Detector 6 in Figure 1 of Murata is adapted to compare a first bit value sequence of a received bit stream received from Receiving Circuit 2 to a second bit value sequence from Pattern Generator 4, which is substantially the same as the transmitted bit pattern stream from Pattern Generator 4, to detect a sequence difference between the first and second bit value sequences; Note: the Abstract of Murata teaches that the first bit value sequence of a received bit stream received from Receiving Circuit 2 is generated by Pattern Generator 4); and

a multi-source agreement compliant electrical connector **conveying** the transmitted and received bit streams (Sending and receiving circuits 1 and 2 in Figure 1 of Murata connect electrical circuitry within Tester 10 to various transmission elements outside of Tester 10 including DSU 24 in Figure 1; hence Sending and receiving circuits 1 and 2 in Figure 1 of Murata are a connector; Figure 7 and the preamble to claim 5 in Murata teach that multiple terminal sources, 11, 12, 13..., DSU 24 and Tester 10 are in communication with each other on a single communication path comprising a half-duplex receive bus referred to as an R-line and a half-duplex transmit bus referred to as an T-line;

hence Sending and receiving circuits 1 and 2 in Figure 1 of Murata are a multi-source agreement compliant electrical connector **conveying** the transmitted and received bit streams), wherein the multi-source agreement compliant electrical connector coupled to the bit stream comparison unit, and wherein the multi-source agreement compliant electrical connector directly couples to a multi-source agreement compliant device (col. 1, lines 26-47 in Murata teach that DSU 24 in Figures 1, 2 and 7 is connected to receive and transmit data to multiple terminal sources 11, 12, 13..., and tester 10; hence DSU 24 is a multi-source agreement compliant device directly coupled to the multi-source agreement compliant electrical connector, Sending and receiving circuits 1 and 2).

The Applicant contends, "As the applicants describe at page 3, lines 24-28 of the originally filed specification, the multi-source agreement compliant device directly couples to the multi-source agreement compliant connection without requiring a plurality of cables, wires, etc."

The Examiner asserts that the multi-source agreement compliant device DSU 24 in Figures 1, 2 and 7 of Murata directly couples to multiple terminal sources 11, 12, 13..., and tester 10 on a singe R-line for receiving and single T-line for transmitting providing a single duplex communication path between up to 8 terminal and DSU 24 with out the need for a separate R-line and T-line for each terminal, the is the R-line and T-line is shared between all devices connected to the R-line and T-line; hence DSU 24 is a multi-source agreement compliant device coupled to the multi-source agreement compliant connection, Sending

and receiving circuits 1 and 2 in Figure 1 of Murata, without requiring a plurality of T-line cables or lines for receiving nor requiring a plurality of R-line cables or lines for transmitting, that is, device communication takes place on a single shared data bus comprising an R-line and a T-line without requiring more than one data bus for communication.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1- are rejected under 35 U.S.C. 102(b) as being anticipated by Murata; Yazuru (US 5099480 A).

35 U.S.C. 102(b) rejection of claim 1.

Murata teaches a bit stream comparison unit **that compares** a first bit value sequence of the received bit stream to a second bit value sequence associated with a transmitted bit stream to detect a sequence difference between the first and second bit value sequences (the Abstract in Murata teaches that the Error Detector 6 in Figure 1 of Murata is adapted to compare a first bit value sequence of a received bit stream received from Receiving Circuit 2 to a second bit value sequence from Pattern Generator 4, which is substantially the same as the

transmitted bit pattern stream from Pattern Generator 4, to detect a sequence difference between the first and second bit value sequences; Note: the Abstract of Murata teaches that the first bit value sequence of a received bit stream received from Receiving Circuit 2 is generated by Pattern Generator 4); and a multi-source agreement compliant electrical connector **conveying** the transmitted and received bit streams (Sending and receiving circuits 1 and 2 in Figure 1 of Murata connect electrical circuitry within Tester 10 to various transmission elements outside of Tester 10 including DSU 24 in Figure 1; hence Sending and receiving circuits 1 and 2 in Figure 1 of Murata are a connector; Figure 7 and the preamble to claim 5 in Murata teach that multiple terminal sources, 11, 12, 13..., DSU 24 and Tester 10 are in communication with each other on a single communication path comprising a half-duplex receive bus referred to as an R-line and a half-duplex transmit bus referred to as an T-line; hence Sending and receiving circuits 1 and 2 in Figure 1 of Murata are a multi-source agreement compliant electrical connector **conveying** the transmitted and received bit streams), wherein the multi-source agreement compliant electrical connector coupled to the bit stream comparison unit, and wherein the multi-source agreement compliant electrical connector directly couples to a multi-source agreement compliant device (col. 1, lines 26-47 in Murata teach that DSU 24 in Figures 1, 2 and 7 is connected to receive and transmit data to multiple terminal sources 11, 12, 13..., and tester 10; hence DSU 24 is a multi-source agreement compliant device directly coupled to the multi-source agreement compliant electrical connector, Sending and receiving circuits 1 and 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata; Yazuru (US 5099480 A).

35 U.S.C. 103(a) rejection of claims 2 and 3.

Murata substantially teaches the claimed invention described in claim 1 (as rejected above).

However Murata does not explicitly teach the specific use of an IC or a printed circuit board.

The Examiner asserts that Murata teaches circuitry for implementing all the elements of claim 1 for ISDN, but does not specify how the circuit is arranged on

a semiconductor or a printed circuit board typically found on an ISDN network device, but instead leaves such obvious features for the design phase of implementing the device taught in Murada to allow the designer flexibility to select from readily available circuitry to implement the design. Note: it is well known in the Art that use of circuit boards allow the designer flexibility to select from readily available circuitry whereas placing all the circuitry on a single semiconductor chip provides a speed-up.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Murata by including use of an IC or a printed circuit board. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an IC or a printed circuit board would have provided flexibility to select from readily available circuitry whereas placing all the circuitry on a single semiconductor chip provides a speed-up.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata; Yazuru (US 5099480 A) in view of Debany, Jr.; Warren H. et al. (US 4580274 A, hereafter referred to as Debany).

35 U.S.C. 103(a) rejection of claim 4.

Murata substantially teaches the claimed invention described in claim 1 (as rejected above).

However Murata does not explicitly teach the specific use of an optical transceiver.

Debany, in an analogous art, teaches use of an optical transceiver (col. 1, lines 50-53 in Debany).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Murata with the teachings of Debany by including use of an optical transceiver. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an optical transceiver would have provided the ability to do loopback testing in a fiber networked environment (Note: optical communication lines are commonly used in ISDN networking environments).

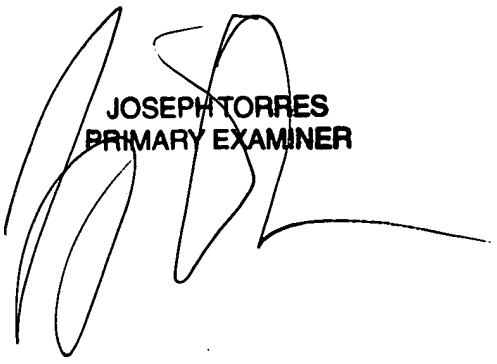
Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Primary Examiner
Art Unit 2133